In re Patent Application of:
FRANCIS ET AL.
Serial No. **10/008,586**
Filing Date: **NOVEMBER 5, 2001**
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In the Claims:

Claims 1 to 11 (Cancelled).

12. (Currently Amended) A system-on-chip (SOC) comprising:

a plurality of circuit blocks, each responsive to a respective local clock signal;

at least one system clock connected to said circuit blocks for providing a system clock signal thereto for functioning as the respective local clock signals;

a power control manager connected to said circuit blocks via respective clock enable lines for selectively providing a shutdown signal ~~thereto;~~ thereto, said power control manager comprising at least one register connected to the respective clock enable lines for storing data indicating logic states of the shutdown signals; and

each circuit block comprising a local power control circuit for selectively maintaining the system clock signal as the local clock signal even after receiving the shutdown signal if the circuit block is in an active state when the shutdown signal is received.

13. (Previously Presented) An SOC according to Claim 12, wherein each local power control circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the respective local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state.

Claim 14 (Cancelled.)

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15. (Currently Amended) An SOC according to ~~Claim 14~~ Claim 12, wherein each circuit block further comprises a block logic circuit having a status line connected to said local power control circuit for providing a status signal thereto indicating whether said circuit block is in the active or idle state.

16. (Previously Presented) An SOC according to Claim 15, wherein each local power control circuit comprises a logic circuit having a first input connected to a respective clock enable line, a second input connected to a respective status line, a third input connected to said at least one system clock, and an output for providing the local clock signal based upon logic states of the shutdown signal, the status signal and the system clock signal.

Claim 17 (Cancelled.)

18. (Currently Amended) An SOC according to ~~Claim 17~~ Claim 12, further comprising a central processing unit connected to said power control manager for determining whether each circuit block is in the active or idle state by querying said at least one register.

19. (Previously Presented) An SOC according to Claim 12, wherein said at least one system clock comprises a plurality of system clocks, each system clock for providing the system clock signal to selected circuit blocks.

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20. (Currently Amended) A system-on-chip (SOC) comprising:

a plurality of circuit blocks;

a system clock connected to said circuit blocks for providing a system clock signal thereto; and

a power control manager connected to said circuit blocks for selectively providing a shutdown signal thereto;

each circuit block comprising

a block logic circuit providing a status signal indicating whether said circuit block is in an active or idle state, and

a local power control circuit for selectively maintaining the system clock signal as a local clock signal even after receiving the shutdown signal if the status signal indicates said circuit block is in the active state when the shutdown signal is ~~receieved.~~ received; and

said power control manager being connected to each local power control circuit through a respective clock enable line for providing the shutdown signal thereto, and comprising at least one register connected to the respective clock enable lines for storing data indicating logic states of the shutdown signals.

21. (Previously Presented) An SOC according to Claim 20, wherein each local power control circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the local clock signal if said corresponding circuit block receiving the shutdown signal is in an idle state.

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Claim 22 (Cancelled.)

23. (Currently Amended) An SOC according to ~~Claim 22~~ Claim 20, wherein each local power control circuit comprises a logic circuit having a first input connected to a respective clock enable line, a second input connected to a respective status line, a third input connected to said system clock, and an output for providing the local clock signal based upon logic states of the shutdown signal, the status signal and the system clock signal.

Claim 24 (Cancelled.)

25. (Currently Amended) An SOC according to ~~Claim 24~~ Claim 20, further comprising a central processing unit connected to said power control manager for determining whether each circuit block is in the active or idle state by querying said at least one register.

26. (Previously Presented) A system-on-chip (SOC) comprising:

a plurality of circuit blocks;

a system clock connected to said circuit blocks for providing a system clock signal thereto;

a power control manager connected to said circuit blocks through a respective clock enable line for selectively providing a shutdown signal thereto, said power control manager comprising at least one register connected to the clock enable lines for storing data indicating logic states of

the shutdown signals;

a central processing unit connected to said power control manager for determining whether each circuit block is in an active or idle state by querying said at least one register; and

each circuit block comprising a local power control circuit for selectively maintaining the system clock signal as a local clock signal even after receiving the shutdown signal if the circuit block is in the active state when the shutdown signal is received.

27. (Previously Presented) An SOC according to Claim 26, wherein each local power control circuit comprises a clock separation circuit connected to said power control manager for preventing the system clock signal from functioning as the local clock signal if said corresponding circuit block receiving the shutdown signal is in the idle state.

28. (Previously Presented) An SOC according to Claim 26, wherein said power control manager is connected to each local power control circuit through the respective clock enable line for providing the shutdown signal thereto.

29. (Previously Presented) An SOC according to Claim 26, wherein each circuit block further comprises a block logic circuit having a status line connected to said local power control circuit for
providing a status signal thereto indicating whether said circuit block is in the active or idle state.

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30. (Previously Presented) An SOC according to Claim 29, wherein each local power control circuit comprises a logic circuit having a first input connected to a respective clock enable line, a second input connected to a respective status line, a third input connected to said system clock, and an output for providing the local clock signal based upon logic states of the shutdown signal, the status signal and the system clock signal.

31. (Currently Amended) A method for powering down circuit blocks within a system-on-chip (SOC) comprising a plurality of circuit blocks, with each circuit block comprising a local power control circuit, the SOC further comprising a power control manager comprising at least one register, the method comprising:

providing a system clock signal to the circuit blocks for functioning as a respective local clock signal;

selectively providing a respective shutdown signal from the power control manager to the local power control circuit in one of the circuit blocks via a respective clock enable line connected therebetween; ~~circuit blocks;~~ and

selectively maintaining the system clock signal as the respective local clock signal ~~block~~ even after receiving the shutdown signal if the circuit block is in an active state when the shutdown signal is ~~received.~~ received; and

storing data in the at least one register indicating logic states of the respective shutdown signals.

32. (Previously Presented) A method according to Claim 31, further comprising preventing the system clock

signal from functioning as the respective local clock signal if the corresponding circuit block receiving the shutdown signal is in an idle state.

Claim 33 (Cancelled.)

34. (Currently Amended) A method according to ~~Claim 33~~ Claim 31, wherein each circuit block further comprises a block logic circuit having a status line connected to the local power control circuit for providing a status signal thereto indicating whether the circuit block is in the active or idle state.

35. (Previously Presented) A method according to Claim 34, wherein each local power control circuit comprises a logic circuit having a first input connected to a respective clock enable line, a second input connected to a respective status line, a third input connected to a system clock, and an output for providing the respective local clock signal based upon logic states of the shutdown signal, the status signal and the system clock signal.

Claim 36 (Cancelled.)

37. (Currently Amended) A method according to ~~Claim 36~~ Claim 31, further comprising querying the at least one register for determining whether each circuit block is in the active or idle state.